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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/665,366	09/19/2000	Douglas O. Powell	EN9-99-026	5058

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EXAMINER	
COMPTON, ERIC B	
ART UNIT	PAPER NUMBER
3726	

DATE MAILED: 01/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/665,366	POWELL, DOUGLAS O.	
	Examiner	Art Unit	
	Eric B. Compton	3726	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-80* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-45 and 68-79* is/are allowed.

6)☒ Claim(s) *46-67 and 80* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 12, 2004, has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 46-48, 51-53, and 64-78, and 80, are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,744,758 to Takenouchi et al in view of U.S. Patent 5,837,119 to Kang et al ("Kang") and U.S. Patent 5,635,010 to Pepe et al ("Pepe").

Takenouchi et al disclose a multi-layered electronic structure and a method for making said structure (see Figures 7(a)-7(e), 8, & 9), comprising the steps of:

a. Providing a plurality of sub-composites (12) comprising: providing a layer of dielectric material (14,16) having a top and bottom;

b. providing a layer of electrically conducting material (13) on one of the top surface of the dielectric layer;

c. forming at least one passage (18) through the dielectric layer;

d. depositing electrically conducting material (32, 34) in at least one of the at least one passage through the dielectric layer;

e. removing portions of the layer of electrically conducting material to define a pattern of circuitry (see Figures 7(d) and 7(e));

f. stacking a plurality of sub-composites (Figure 9);

g. aligning the plurality of sub-composites (it is inherent that the structures are aligned);

h. joining the plurality of sub-composites such that the electrically conducting material in at least one on the at least one the blind vias makes electrically contact by forming a metallurgical bond (see col. 10, lines 65-67) to the conductive pattern (by heat press, col 11, lines 63-65); and

i. filling the spaces between adjacent sub-composites with electrically insulating material (via heat pressing, see Figure 8).

However, Takenouchi et al do not disclose that conductive paste forms a metallurgical bond.

Kang discloses a conductive paste of the type disclosed by both Takenouchi and Applicant "for forming electroconductive connections between electroconductive members and methods of use in electronic applications." Col. 1, lines 10-13; *see also* Figure 2B. The reference further discloses

According to an embodiment of the present invention, ***an electrically conductive paste (ECP) material is disclosed***, which consists of copper powder coated with a thin layer of low melting point, Pb-free metals, such as Sn, In, Bi, Sb and their alloys, mixed with an environmentally-safe fluxing agent, and dispersed in the matrix of thermoplastic or thermosetting polymers. The microstructure of the ECP containing Sn-coated Cu powder is shown in its cross-section view in FIG. 3.

In one particular embodiment, we disclose a new electrically conductive paste material consisting of indium-coated copper powder, polyimide-siloxane, solvent (NMP), no clean flux, and carboxylic acid/surfactant. The indium-coated copper powder is produced by a sequential electrodeposition of copper dendrite powder on a dummy substrate, followed by another electrodeposition of indium on the copper dendrite powder. The copper dendrite powder can be replaced by other dendritic powders such as nickel, cobalt, chromium, palladium, platinum, and others. The indium can be replaced by other metals such as Sn, Zn, Pb, Bi and Sb or their alloys. Because the dendritic powder has a large aspect ratio, it has an advantage of better electrical and/or thermal conduction characteristics in comparison to the spherical powder. ***A joining operation can be performed near the melting point of In, 157.degree. C., where a metallurgical bonding of In-to-In or In-to-Au or In-to-Cu is accomplished at the dendritic particle-to-particle as well as dendritic particle-to-substrate pad interfaces***. Since indium metal and alloys have an excellent wetability on the metals that are hard to solder to, such as aluminum, titanium, molybdenum, or tungsten, the present invention material can be used for joining of liquid crystal display devices. The joining process can be either solid-state or liquid-solid reaction. The polymer curing process can be combined with the joining process depending on the paste formulation. ***Because of the metallurgical bonding and the high conductivity copper core, a higher electrical conductivity is expected with the joints made of the new paste material than with those of the silver-epoxy material. The metallurgical bonds also provide stable electrical conductivity of the new joints upon thermal exposure and cycling. It is also expected to have a higher joint strength from the combined effect of the metallurgical and adhesive bonds.***

Col. 4, line 35 – Col. 5, line 9 (emphasis added).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have formed the multi-layered electronic structure by the method of Takenouchi et al using a conductive paste capable of forming metallurgical bonds, in light of the teachings of Kang, in order to provide a more reliable bonds

resistant to high thermal cycling. The reference teaches applying the resin as in its un-cured state as a liquid. *See* Col.6, lines 27-33 ("Desirably, the adhesive will exhibit viscous flow under the applied pressure at temperatures which are below its curing temperature, e.g., at temperatures from about 200 ° C to 300 ° C., and which will cure to a solid adhesive layer at more elevated temperatures, e.g., from about 300 ° C to 400 °C."). Once applied the resin is solidified by a curing process. *See* Col. 8, lines 40-42 ("The stack 122 is maintained under pressure and temperature for sufficient time to cure the adhesive layer and then is cooled.").

Takenouchi et al/Kang disclose the invention cited above. The reference relies on pressure and heat to bond the structures. However, it does not specifically disclose providing filling the spacing between adjacent structures with a un-cured liquid, which is transformed into a solid by curing.

Pepe discloses a method for bonding layers to form a laminate (see Figures 9-12). A dielectric adhesive, preferably a polyimide, applied as a liquid is provided to close voids and help bond substrates together. "The preferred polyimide exhibits sufficient viscous flow at the initial temperature and pressure conditions such that it fills all voids between adjacent chips and excess adhesive extrudes from the chip stack to achieve minimal thickness of the adhesive layer." Col 7, lines 58-63. "As shown in FIG. 7, layer 70 of insulation (polyimide of SiON)) has been deposited over the entire upper (device) surface on the wafer 20." Col. 4, lines 42-44. "In forming the polyimide layer 70, polyimide material ***in liquid form is spun on***, sprayed on, or otherwise caused to cover the surface of the wafer." Col. 4, lines 51-53 (emphasis added). "***After the layer has***

been applied in liquid form, it is heated to remove solvent, which constitutes about 74 weight percent of the applied liquid ***and cured***." Col. 4, lines 58-60 (emphasis added).

Regarding claim 46, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have provided a liquid insulator to bond the structures of Takenouchi et al/Kang, in light of the teachings of Pepe, in order to fill the voids between the structures.

Regarding claims 66 and 67, an electronic package, formed by the method above is shown and described. Furthermore, it is inherent that such structures are used for mounting electrical components.

Regarding claims 47-48, Takenouchi al disclose that the dielectric layer (16) may be polyimide (col 6, line 4)

Regarding claims 51-52, Takenouchi et al disclose that the conducting material is copper foil (col 10, line 30).

Regarding claim 53, Takenouchi et al disclose that the conducting material is a metal deposited in the passages in by platting (col 10, line 5).

Regarding claim 64, and 65, Takenouchi et al inherently disclose that the structures are filled with a thermoset plastic (16, see col 12, lines 3-5).

4. Claims 49-50, 54-58, and 60-63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takenouchi et al/Kang/Pepe in view of US Patent 4,915,983 to Lake et al.

Takenouchi et al/ Kang/Pepe disclose the invention cited above. However, they do not disclose the particulars of the invention as claimed by Applicant.

Lake et al disclose a multi-layered electronic structure and a method for making said structure (see Figure 8) very similar in structure to both Takenouchi et al and Applicant's inventions. Many of the particulars not disclosed by Takenouchi et al are disclosed Lake et al, which are apparently all in the art of forming interconnects.

Regarding claims 49-50, 54-58, and 60-63, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have formed the sub-composites of Takenouchi et al/Kang/Pepe using the various interconnect forming techniques well-known in the art, in light of the teachings of Lake et al, in order to take advantage of well-known interconnect forming technology, thus saving capital costs on retooling production lines for new product runs.

Regarding claim 49, Official Notice is taken that liquid crystal polymer film is well known in the circuit board arts and a skilled artisan would have found it obvious at time of invention to use such in the method of Takenouchi et al/Kang/Pepe.

Regarding claim 50, Lake et al disclose that the dielectric (50) may be polyimide (col 9, line 33) and/or include a mesh or screen of glass (col 10, lines 37-38).

Regarding claims 54, 55, and 56, Lake et al disclose a layer of tin lead alloy may be applied over the copper foil by a continuous electroplating process (col 9, lines 57-59).

Regarding claim 57, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have provide a cap having a thickness of

0.0001 to .0004 inch, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claims 60-62, Official Notice is taken that aligning structure such as providing holes in the laminate layers and a jig having corresponding aligning pins and indicia (registration marks) are well known in the art. Applicant, also alludes to the fact such structures are known, referring to slots and pins as standard alignment means (page 34, lines 2-3).

Regarding claim 63, Lake et al disclose that the layers will be soldered coated (col 9, line 39).

Regarding claim 58, Official Notice is taken that coating a substrate with oxides (e.g. tin oxide) are known in the art to roughen the surface for subsequent bonding and a skilled artisan would have found it obvious at time of invention to apply a coating for such purpose.

Allowable Subject Matter

5. Claims 1-45 and 68-79 are allowed.

6. Independent claims 1 and 68 define over the prior art of record. Applicant's remarks regarding the prior art in the response dated November 12, 2004, have been found persuasive especially with respect to Pepe. Pepe does not disclose, "flowing an

un-cured resin into said voids" nor "filling the space between adjacent structures with an uncured resin," once the structures are aligning and joined, as required for these claims.

7. U.S. Pat. 5,376,326 to Medney et al discloses a similar invention. *See* Figures 19-20; Cols. 23-25. However, as shown in Figure 19C2, a spreader block (414) is used to spread the layers prior to injection of the resin. Thus, the step of forming a mechanical bond and electrical contact between adjacent structures is not provided for.

Response to Arguments

8. Applicant's arguments with respect to the claims have been considered but are not found fully persuasive.

9. Independent claims 1 and 68 have been allowed.

10. Applicant's amendment failed to amend independent claims 46, and 66-67, directed to a parallel joining technology.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Compton whose telephone number is (571) 272-4527. The examiner can normally be reached on M-F, 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter B. Vo can be reached on (571) 272-4690. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric Compton
Patent Examiner